Brief information about the project

Name of the project	AP09058525 «Development of 5G digital radio modules and microwave signal receiving stations based on SoC»
Relevance	The radio unit must be made in a modular format so that each module is connected via a standard interface such as PCIe. RU consists of RF interface, digital interface, Ethernet transport, synchronization, and processing of the baseband of the lower layer PHY. Accordingly, the lower PHY processing will be performed on the FPGA. Xilinx's modern system on a chip (SoC), RFSoC, consists of an FPGA with ARM processors, ADCs and DACs, all on a single chip. The technology has over 16 nm 4200 DSP cuts; four A53 ARM processors with a clock speed of 1.5 GHz; two 600 MHz R5 ARM processors; Eight 4 GHz, 12-bit ADCs and eight 6.4 GHz, 14-bit DACs per device. The above characteristics of the modern SoC from Xilinx are well suited for the development of digital low-level processing blocks, which include FFT / iFFT functions, CP addition, PRACH and digital beamforming. The RF interface consists of antenna elements, bandpass filters, power amplifiers, low noise amplifiers, digital analog converters, and analog digital converters. The digital interface consists of digital up-converter, digital downconverter, digital predistortion, and crest factor reduction. A prerequisite for the development of this project is the experienced and previously created radio transmitting devices, coding algorithms, generators of complex nonlinear signals and other digital devices based on FPGAs, new proposed digital filter models, which will be discussed in more detail in the following sections, numerous copyright certificates and patents of participants in this project on multiband antenna devices, information security systems based on FPGAs, as well as processing big data using deep learning neural networks and broadband signal generators
Purpose	The main goal of this project is to develop 5G radio modules, which consist of an RF amplifier, converters, receiving, filtering and other digital blocks, based on modern high-performance systems on a single chip (RFSoC), using parallel computation methods in Field-Programmable Gate Array.
Objectives	To achieve the intended aim, the following project objectives were identified: The first objective includes the development of an algorithm for a separate RU based on FPGA Xilinx with the possibility of further integration with the CU-DU. The second objective is to write programs for individual digital blocks of 5G radio modules in Verilog HDL language. The third objective is to test the algorithm for the operation of individual digital blocks of the radio module in the Verilog Testbench software environment and to optimize the algorithm through parallel computation of several information streams. The fourth objective is to debug the digital radio module on modern systems on a single chip.

	The fifth objective is to test the completed prototype 5G digital radio on the SoC. The sixth objective is to analyze and test the speed of data exchange and processing, as well as data coding and storage when integrating an industrial design with the core entral module of a 5G mobile network.
Expected and achieved results	Results obtained and novelty: In this work, a cluster router was proposed that performs fast route construction by clustering the network based on eccentricity, which ensures device autonomy in case of failures. This router, unlike other routers based on Dijkstra's algorithm, builds a route first between clusters and then between network nodes, which allows it to significantly improve data transfer speeds in 5 G technologies . In addition, to divide the network, we used the CIEA algorithm we developed , which has the closest results to theoretical results. To analyze this router based on CIEA , we calculated the Tsallis and Rényi network information dimensions of the UV-flower model using box coverage algorithms. As is known, fractal networks have better coverage and connectivity than non-fractal networks. Therefore, fractal networks like UV- flower are better suited for constructing a topology for 5 G. Application and efficiency: The developed 5 G radio modules based on SoC and FPGA are focused on the domestic production of individual physical modules of telecommunication systems.
Research team members with their identifiers (Scopus Author ID, Researcher ID, ORCID, if available) and links to relevant profiles	Ibraimov Margulan Kassenovich, PhD, *h*-индекс – 4, ORCID: 0000-0002-8049-3911 Scopus Author ID: 57196373551 Kozhagulov Yeldos, PhD, *h*-индекс – 2, ORCID: 0000-0001-5714-832X, Scopus Author ID: 57192878535
List of publications with links to them	Скабылов А., Ибраимов М., Жексебай Д., Кожагулов Е. ПРОГРАММНО-АППАРАТНАЯ РЕАЛИЗАЦИЯ QPSK НА БАЗЕ ZYNQ И MATLAB //Вестник «Физико-математические науки». – 2022. – Т. 77. – №. 1. – С. 146-150. DOI:https://doi.org/10.51889/2022-1.1728-7901.20. Ibraimov M.K., Tynymbayev, S.T., Skabylov, A.A., Kozhagulov, Y., Zhexebay, D.M. Development and design of an FPGA-based encoder for NPN //Cogent Engineering. – 2022. – V. 9. – №. 1. – P. 2008847, Q2, CiteScore =68%. https://www.scopus.com/authid/detail.uri?authorId=57189617696 Akhtanov, S., Turlykozhayeva, D., Ussipov, N., Ibraimov M., Zhanabaev, Z.. Centre including eccentricity algorithm for complex networks //Electronics Letters. – 2022. – V. 58. – №. 7. – P. 283-285, Q2, CiteScore =55%. https://www.scopus.com/authid/detail.uri?authorId=57189617696 Zhanabaev Z., Akhtanov S., Turlykozhaeva D., Ussipov N., Ibraimov M. CLUSTER ROUTER BASED ON ECCENTRICITY //Eurasian Physical Technical Journal. – 2022. – V. 19. – №. 3 (41). – P. 84-90. CiteScore =25%. DOI 10.31489/2022No3/84-90 Ибраимов М.К., Кожагулов Е.Т, Жексебай Д.М., Дәулетова А.Н., Файзрахман Ә.Қ. ZYNQ және MATLAB негізінде QPSK

	таратып-қабылдағышының бағдарламалық-ақпараттық іске асырылуы // «Бейсызық жүйелердегі хаос және құрылымдар. Теория және тәжірибе» XII Халықаралық ғылыми конференция материалдары, - Павлодар, 2022. - Б.172-178. Ахтанов С. Н., Ибраимов М. К., Турлыкожаева Д., Усипов Н.М. Кластерная маршрутизация фрактальных сетей на основе эксцентриситета // Материалы XII Международной научной конференции «Хаос и структуры в нелинейных системах. теория и эксперимент», - Павлодар, 2022 - С. 213-219.
Patents	Патент 2022/0471.2. Кластерный маршрутизатор на основе эксцентриситета / Ахтанов С.Н, Турлыкожаева Д.А, Үсіпов Н.М, Ибраимов М.К.; заявитель и патентообладатель Ахтанов С.Н, Турлыкожаева Д.А, Үсіпов Н.М, Ибраимов М.К.; 05.08.2019, Бюлл. №31